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EXAMINER	
LEE, ANDREW CHUNG CHEUNG	
ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,947	EVANS ET AL.	
	Examiner	Art Unit	
	Andrew C. Lee	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,5-12 and 21-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,5-12 and 21-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The amendment filed 08/18/2005 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: Regarding claim 21, the subject matters of "an apparatus comprising: a first programmable interconnect matrix having one or more first multiplexers configured to (i) receive a distributed input group of signals in a first order and (ii) present said distributed input group of signals in a second order; and a second programmable interconnect matrix having one or more second multiplexers configured to receive said distributed input group of signals from said first programmable-interconnect matrix in said second order, wherein (i) said first order of said signals are different from said second order of said signals and (ii) said second order of said signals are disposed in an input-reorder channel."; Regarding claim 24, the subject matters of "an apparatus comprising: a first distributed multiplexer configured to generate a first output signal in response to (i) a first portion coupled to a first group of input signals and (ii) a second portion coupled to a second group of input signals; and a second distributed multiplexer configured to generate a second output signal in response to a (i) a first portion coupled to a third group of input signals and (ii) a second portion coupled to a fourth group of input signals, wherein (i) said first portion of said first distributed multiplexer is physically separated from said second portion of said first distributed multiplexer on a layout area and (ii) said first portion of said second distributed multiplexer is physically

separated from said second portion of said second distributed multiplexer on said layout area.'; regarding claim26, the limitation of "the apparatus according to claim 24, wherein (i) said first portion of said second distributed multiplexer and comprises a programmable multiplexer bit coupled to any of said third group of input signals and (ii) said second portion of said second distributed multiplexer comprises a programmable multiplexer bit coupled to any of said fourth group of input signals to allow any of said third or fourth groups of input signals to pass through on said second output signal"; Regarding claim 27, the subject matters of "the apparatus according to claim 24, wherein (i) said first portion of said first distributed multiplexer is separated from said second portion of said first distributed multiplexer on a die and (ii) said first portion of said second distributed multiplexer is separated from said second portion of second distributed multiplexer on a die."

Applicant is required to cancel the new matter in the reply to this Office Action.

2. The disclosure is objected to because of the following informalities:

Regarding claim 27, the term "on a die" is not disclosed and addressed in the original specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 21, 24, 26, 27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one

skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Regarding claim 21, the limitation of "an apparatus comprising: a first programmable interconnect matrix having one or more first multiplexers configured to (i) receive a distributed input group of signals in a first order and (ii) present said distributed input group of signals in a second order; and a second programmable interconnect matrix having one or more second multiplexers configured to receive said distributed input group of signals from said first programmable-interconnect matrix in said second order, wherein (i) said first order of said signals are different from said second order of said signals and (ii) said second order of said signals are disposed in an input-reorder channel."; regarding claim 24, the limitations of "an apparatus comprising:
a first distributed multiplexer configured to generate a first output signal in response to (i) a first portion coupled to a first group of input signals and (ii) a second portion coupled to a second group of input signals; and a second distributed multiplexer configured to generate a second output signal in response to a (i) a first portion coupled to a third group of input signals and (ii) a second portion coupled to a fourth group of input signals, wherein (i) said first portion of said first distributed multiplexer is physically separated from said second portion of said first distributed multiplexer on a layout area and (ii) said first portion of said second distributed multiplexer is physically separated from said second portion of said second distributed multiplexer on said layout area.'; regarding claim26, the limitation of "the apparatus according to claim 24, wherein (i) said first portion of said second distributed multiplexer and comprises a programmable multiplexer bit coupled to any of said third group of input signals and (ii) said second portion of said second distributed multiplexer

comprises a programmable multiplexer bit coupled to any of said fourth group of input signals to allow any of said third or fourth groups of input signals to pass through on said second output signal"; regarding claim 27, the limitation of "the apparatus according to claim 24, wherein (i) said first portion of said first distributed multiplexer is separated from said second portion of said first distributed multiplexer on a die and (ii) said first portion of said second distributed multiplexer is separated from said second portion of second distributed multiplexer on a die."

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims **21**, 22, 23, 2, 5, 6, 7, 8, 9, 10, 11, **24**, 25, 26, 27, 28, 29, 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Nayak (US 6370140 B1).

Regarding claim 21, Nayak discloses the limitation of an apparatus comprising: a first programmable interconnect matrix having one or more first multiplexers configured to (i) receive a distributed input group of signals in a first order (Fig. 1, column 3, lines 44 – 60; Fig. 3, Fig. 6) and (ii) present said distributed input group of signals in a second order (Fig. 1, column 3, lines 51 – 57; Fig. 4, column 5, lines 11 – 20); and a second

programmable interconnect matrix having one or more second multiplexers configured to receive said distributed input group of signals from said first programmable-interconnect matrix in said second order (Fig. 4, column 5, lines 11 – 20; column 6, lines 1 – 12), wherein (i) said first order of said signals are different from said second order of said signals (column 9, lines 4 – 8; lines 52 – 63)and(ii) said second order of said signals are disposed in an input-reorder channel (column 9, lines 26 – 32; lines 46 – 61).

Regarding claim 22, Nayak discloses the limitation of the apparatus according to claim 21, wherein said distributed input group of signals are divided into a first group of input signals and a second group of input signals, wherein said first group of input signals is presented to one of said first multiplexers and said second group of input signals is presented to another of said first multiplexers (Fig. 6, column 9, lines 4 – 14; lines 52 – 54).

Regarding claim 23, Nayak discloses the limitation of the apparatus according to claim 22, wherein any one of said second multiplexers is configured to receive a mix of inputs from said first and second groups of input signals (Fig. 6, elements 612, 618, 604, 608; column 9, lines 4 – 25).

Regarding claim 2, Nayak discloses the limitation of the apparatus according to claim 21, wherein said apparatus comprises a plurality of bits each configured to evenly load said input groups (column 9, lines 10 – 14).

Regarding claim 5, Nayak discloses the limitation of the apparatus according to claim 2, wherein said bits comprise programmable interconnect matrix (PIM) bits (column 9, lines 4 – 14).

Regarding claim 6, Nayak discloses the limitation of the apparatus according to claim 21, wherein said apparatus is configured to provide flexible reprogramming of said first programmable interconnect matrix and second programmable interconnect matrix (column 11, lines 66 – 67; column 12, lines 24 – 36).

Regarding claim 7, Nayak discloses the limitation of the apparatus according to claim 21, wherein said apparatus is scalable (column 11, lines 66 – 67; column 12, lines 1 – 15).

Regarding claim 8, Nayak discloses the limitation of the apparatus according to claim 7, wherein a configuration of said apparatus is expandable in a horizontal direction (column 12, lines 6 – 9).

Regarding claim 9, Nayak discloses the limitation of the apparatus according to claim 8, wherein said configuration of said apparatus is expandable in a vertical direction (Fig. 8, column 12, lines 9 – 23).

Regarding claim 10, Nayak discloses the limitation of the apparatus according to claim 9, wherein said configuration reduces complexity of physical routes of said distributed input groups (column 3, lines 15 – 32; lines 58 – 60).

Regarding claim 11, Nayak discloses the limitation of the apparatus according to claim 21, wherein a layout of said circuit apparatus is deterministic (Fig. 5, column 5, lines 21 – 33; Fig. 7, column 10, lines 34 – 55).

Regarding claim 24, Nayak discloses the limitation of an apparatus comprising: a first distributed multiplexer configured to generate a first output signal in response to (i) a first portion coupled to a first group of input signals (Fig. 6, elements 612, 618, 604; column

9, lines 26 – 32) and (ii) a second portion coupled to a second group of input signals (column 9, lines 28 – 32); and a second distributed multiplexer configured to generate a second output signal in response to a (i) a first portion coupled to a third group of input signals and (ii) a second portion coupled to a fourth group of input signals (Fig. 7, column 10, lines 22 – 50), wherein (i) said first portion of said first distributed multiplexer is physically separated from said second portion of said first distributed multiplexer on a layout area and (ii) said first portion of said second distributed multiplexer is physically separated from said second portion of said second distributed multiplexer on said layout area (column 7, lines 21 – 32).

Regarding claim 25, Nayak discloses the limitation of the apparatus according to claim 24, wherein (i) said first portion of said first distributed multiplexer and comprises a programmable multiplexer bit coupled to any of said first group of input signals (Fig. 6, lines 4 – 11) and (ii) said second portion of said first distributed multiplexer comprises a programmable multiplexer bit coupled to any of said second group of input signals to allow any of said first or second groups of input signals to pass through on said first output signal (Fig. 6, lines 4 – 12; lines 26 – 39).

Regarding claim 26, Nayak discloses the limitation of the apparatus according to claim 24, wherein (i) said first portion of said second distributed multiplexer and comprises a programmable multiplexer bit coupled to any of said third group of input signals (Fig. 6, lines 4 – 11) and (ii) said second portion of said second distributed multiplexer comprises a programmable multiplexer bit coupled to any of said fourth group of input signals to allow

any of said third or fourth groups of input signals to pass through on said second output signal (Fig. 6, lines 4 – 12; lines 26 – 39; lines 46 – 53).

Regarding claim 27, Nayak discloses the limitation of the apparatus according to claim 24, wherein (i) said first portion of said first distributed multiplexer is separated from said second portion of said first distributed multiplexer on a die (column 7, lines 21 – 32; Fig. 1, column 3, lines 44 – 51; Fig. 6, elements 604, 608) and (ii) said first portion of said second distributed multiplexer is separated from said second portion of second distributed multiplexer on a die (Fig. 6, elements 604, 608; column 4, lines 29 – 35).

Regarding claim 28, Nayak discloses the limitation of the apparatus according to claim 24, further comprising a programmable interconnect matrix configured to be expanded or contracted to implement any number of distributed multiplexers (column 11, lines 66 – 67, scalability, column 12, lines 1 – 15).

Regarding claim 29, Nayak discloses the limitation of the apparatus according to claim 24, wherein said apparatus provides (i) a deterministic layout area and (ii) an input grouping configuration which allows said first and second groups of input signals to remain consistent across any number of distributive multiplexers (column 12, claim 1, lines 45 – 62).

Regarding claim 30, Nayak discloses the limitation of the apparatus according to claim 24, wherein a plurality of said first distributed multiplexers and a plurality of said second distributed multiplexers are implemented as a programmable interconnect matrix (Fig. 3, column 4, lines 58 – 65).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nayak (US 6370140 B1) in view of Agrawal et al. (US 5015884).

Regarding claim 12, Nayak discloses the limitation of an apparatus comprising: a first programmable interconnect matrix having one or more first multiplexers, Nayak does not disclose expressly the apparatus according to claim 21, wherein a delay of said apparatus is deterministic. Agrawal et al. disclose the limitation of the apparatus according to claim 21, wherein a delay of said apparatus is deterministic (column 13, lines 23 – 25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Nayak to include an apparatus according to claim 21, wherein a delay of said apparatus is deterministic such as that taught by. Agrawal et al. in order to provide a fixed, uniform, predictable and path independent time delay for all signals that are passed through the switch matrix (as suggested by Agrawal et al. see column 6, lines 43 – 46).

Response to Arguments

8. Applicant's arguments with respect to claims 2,5-12 and 21-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571) 272-3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (571) 272-3134. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ACL Nov 20, 2005

Ajit Patel
Primary Examiner